# ABSTRACT

A step-down circuit is provided that comprises a clock control circuit which provides a plurality of clock signals having a frequency determined based on a control signal; a charge pump circuit which reduces a first potential applied to a first terminal and then provides a second potential from a second terminal by switching the connection of a plurality of capacitors in sync with a plurality of the clock signals output from the clock control circuit; and a comparator which produces the control signal to be supplied to the clock control circuit by comparing the second potential to a reference potential.